Chapter

9 Logic gates

Learning Summary

In this chapter you will learn about:

- ***Logic gates***
- ***Truth tables***
- ***Logic circuits/networks***

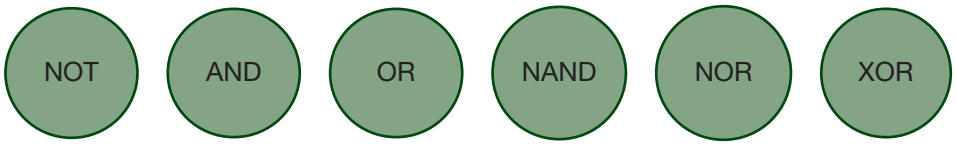
In this chapter we will look at how logic gates are used and how truth tables are used to check if combinations of logic gates (known as logic circuits or logic networks) carry out the required functions.

9.1 Logic gates

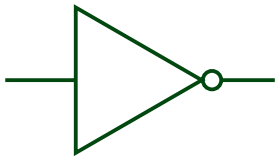
Signals can be represented as ON or OFF, 1 or 0 as well.

A large number of electronic circuits (in computers, control units, and so on) are made up of logic gates. These process signals which represent true or false.

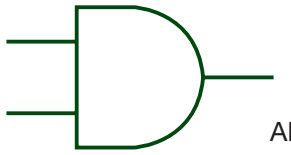
The most common symbols used to represent logic gates are shown below. In this book, we will use the ***MIL symbols***. But the reader may also see the simpler, more general, logic gate representations.



MIL symbols

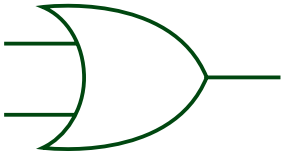


NOT gate

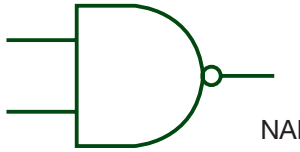


AND gate

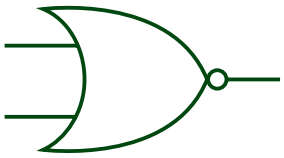
There are many different logic gates but we will concentrate on these.

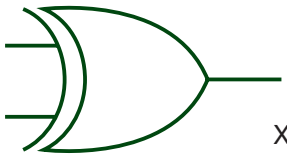


OR gate



NAND gate


NOR gate


XOR gate

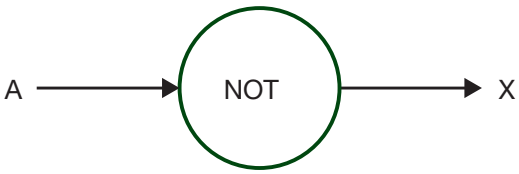
9.2 Truth tables

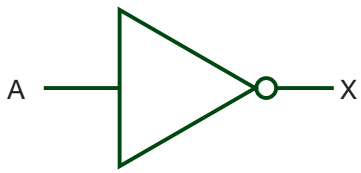
Truth tables are used to show logic gate functions. The NOT gate has only one input, but all the others have two inputs.

When constructing a truth table, the binary values 1 and 0 are used. Every possible combination, depending on number of inputs, is produced. Basically, the number of possible combinations of 1s and 0s is 2^n where n = number of inputs. For example, 2 inputs have 2^2 combinations (i.e. 4), 3 inputs have 2^3 combinations (i.e. 8) and so on. The next section shows how these truth tables are used.

Description of the six logic gates

NOT gate





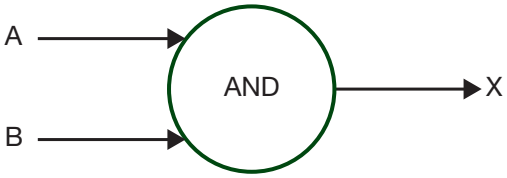
The output (X) is **true** (i.e. 1 or ON) if:

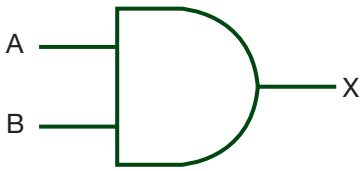
INPUT A is **NOT TRUE** (i.e. 0 or OFF)

Truth table for: ***X = NOT A***

INPUT A	OUTPUT X
0	1
1	0

AND gate





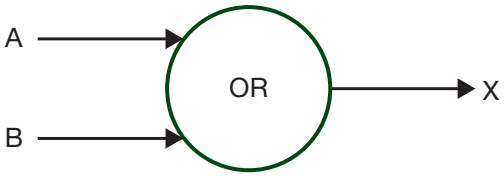
The output (X) is **true** (i.e. 1 or ON) if:

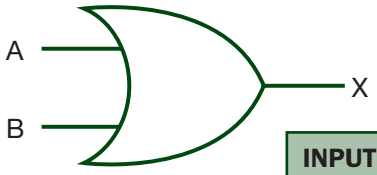
INPUT A AND INPUT B are **BOTH TRUE** (i.e. 1 or ON)

Truth table for: ***X = A AND B***

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	0
1	0	0
1	1	1

OR gate





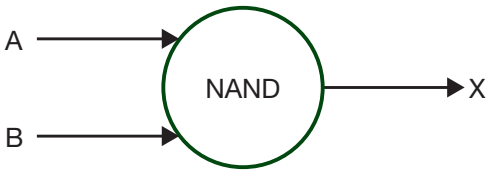
INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	1

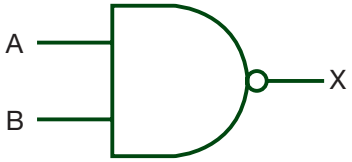
The output (X) is **true** (i.e. 1 or ON) if:

INPUT A OR INPUT B is **TRUE** (i.e. 1 or ON)

Truth table for: ***X = A OR B***

NAND gate





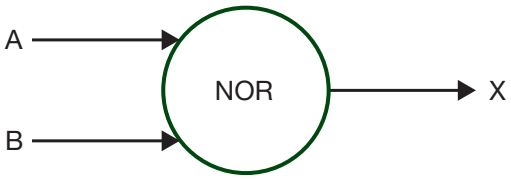
INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	1
1	0	1
1	1	0

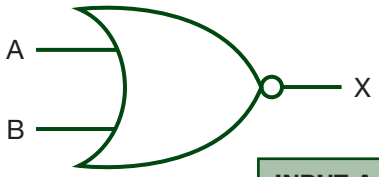
The output (X) is **true** (i.e. 1 or ON) if:

INPUT A AND INPUT B are **NOT BOTH TRUE** (i.e. 1 or ON)

Truth table for: ***X = NOT A AND B***

NOR gate





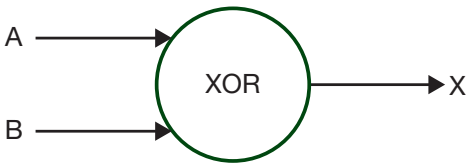
INPUT A	INPUT B	OUTPUT X
0	0	1
0	1	0
1	0	0
1	1	0

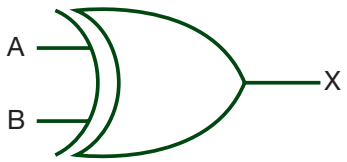
The output (X) is **true** (i.e. 1 or ON) if:

INPUT A OR INPUT B are **NOT BOTH TRUE** (i.e. 1 or ON)

Truth table for: ***X = NOT A OR B***

XOR gate





The output (X) is **true** (i.e. 1 or ON) if:

INPUT A OR (NOT INPUT B) OR (NOT INPUT A) OR INPUT B

is **TRUE** (i.e. 1 or ON)

Truth table for: ***X = A OR (NOT B) OR (NOT A) OR B***

INPUT A	INPUT B	OUTPUT X
0	0	0
0	1	1
1	0	1
1	1	0

9.3 Logic circuits/networks

Logic gates can be combined together to produce more complex logic circuits (networks).

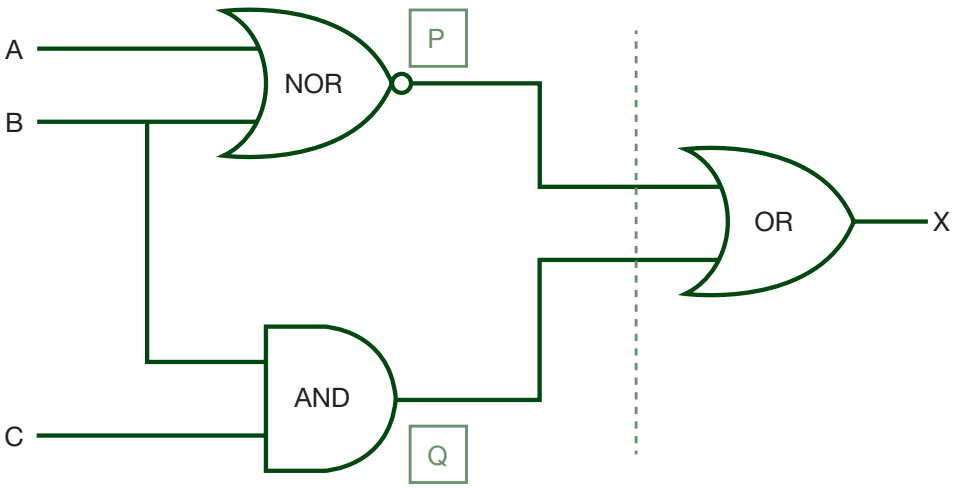
Key Point **The output from a logic circuit (network) is checked by producing a truth table.**

Two different types of problem are considered here:

- drawing the truth table from a given logic circuit (network)
- designing a logic circuit (network) from a given problem and testing it by also drawing a truth table.

Example 1

Produce a truth table from the following logic circuit (network).



To show how this works, we will split the logic circuit into two parts (shown by the dotted line).

First part

There are 3 inputs; thus we must have 2^3 (i.e. 8) possible combinations of 1s and 0s.

To find the values (outputs) at points **P** and **Q**, it is necessary to consider the truth tables for the NOR gate (output P) and the AND gate (output Q) i.e.

P = A **NOR** B
Q = B **AND** C

We thus get:

INPUT A	INPUT B	INPUT C	OUTPUT P	OUTPUT Q
0	0	0	*1*	*0*
0	0	1	*1*	*0*
0	1	0	*0*	*0*
0	1	1	*0*	*1*
1	0	0	*0*	*0*
1	0	1	*0*	*0*
1	1	0	*0*	*0*
1	1	1	*0*	*1*

Second part

There are 8 values from **P** and **Q** which form the inputs to the last **OR** gate.

Hence we get X = P **OR** Q which gives the following truth table:

INPUT P	INPUT Q	OUTPUT X
1	0	*1*
1	0	*1*
0	0	*0*
0	1	*1*
0	0	*0*
0	0	*0*
0	0	*0*
0	1	*1*

Which now gives us the final truth table for the logic circuit given at the start of the example:

INPUT A	INPUT B	INPUT C	OUTPUT X
0	0	0	*1*
0	0	1	*1*
0	1	0	*0*
0	1	1	*1*
1	0	0	*0*
1	0	1	*0*
1	1	0	*0*
1	1	1	*1*

Example 2

Consider the following problem.

A system used 3 switches A, B and C; a combination of switches determines whether an alarm, X, sounds:

If switch A or switch B are in the ON position and if switch C is in the OFF position then a signal to sound an alarm, X is produced.

Remembering that ON = 1 and OFF = 0; also remember that we write 0 as NOT 1.

It is possible to convert this problem into a logic statement.

So we get:

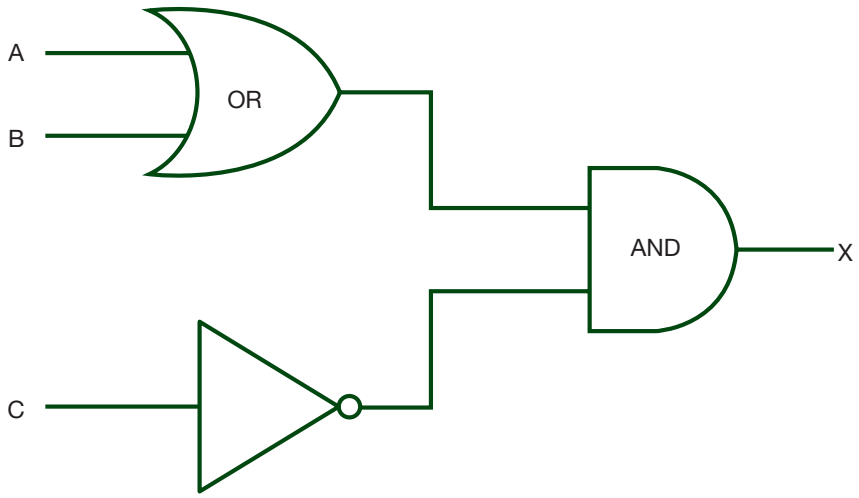
If (A = 1 **OR** B = 1) **AND** (C = **NOT** 1) then X = 1

The first part is two inputs (A and B) joined by an **OR** gate

The output from the first part and the third part are joined by an **AND** gate

The third part is one input (C) which is put through a **NOT** gate

So we get the following logic circuit (network):



This gives the following truth table:

INPUT A	INPUT B	INPUT C	OUTPUT X
0	0	0	*0*
0	0	1	*0*
0	1	0	*1*
0	1	1	*0*
1	0	0	*1*
1	0	1	*0*
1	1	0	*1*
1	1	1	*0*

Example 3

A manufacturing process is controlled by a built in logic circuit which is made up of AND, OR and NOT gates only. The process receives a STOP signal (i.e. X = 1) depending on certain conditions, shown in the following table:

INPUTS	BINARY VALUES	CONDITION IN PROCESS
V	1	Volume > 1000 litres
	0	Volume <= 1000 litres
T	1	Temperature > 750°C
	0	Temperature <= 750°C
S	1	Speed > 15 metres/second (m/s)
	0	Speed <= 15 metres/ second (m/s)

A stop signal (X = 1) occurs when:

either Volume, V > 1000 litres and Speed, S <= 15 m/s

or Temperature, T <= 750°C and Speed, S > 15 m/s

Draw the logic circuit and truth table to show all the possible situations when the stop signal could be received.

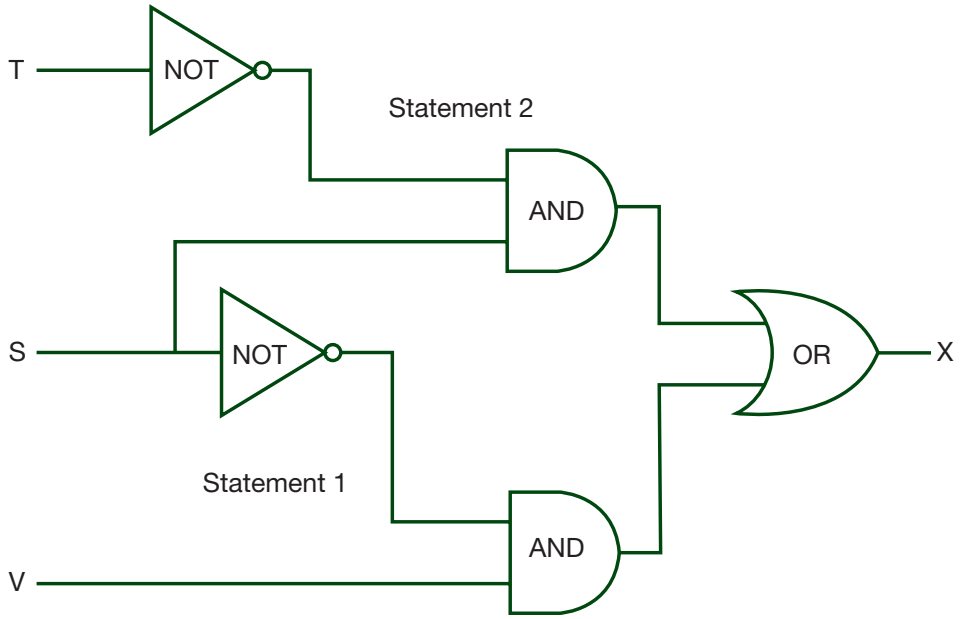
First of all, it is necessary to turn the problem into a series of logic statements:

- statement 1 can now be re-written as:
  V = 1 **AND** S = **NOT** 1 since V > 1000 (binary value = 1) and S <= 15 (binary value = 0)
- statement 2 can now be re-written as:
  T = **NOT** 1 **AND** S = 1 since T <= 750°C (binary value = 0) and S > 15 (binary value = 1)
- both statements are joined together by an **OR gate**

So, our logic statement becomes:
X = 1 if (V = 1 **AND** S = **NOT** 1) **OR** (T = **NOT** 1 **AND** S = 1)

We can now draw the logic circuit (network) by constructing it for statement 1 and for statement 2 and joining them with an **OR** gate.

In the following logic circuit note that V has been placed at the bottom of logic diagram – this is done to avoid crossing over of lines which makes it look neater and less complex. It is not essential to do this and is only done for the reasons given.



We can now construct the truth table:

INPUT V	INPUT T	INPUT S	OUTPUT X
0	0	0	*0*
0	0	1	*1*
0	1	0	*0*
0	1	1	*0*
1	0	0	*1*
1	0	1	*1*
1	1	0	*1*
1	1	1	*0*

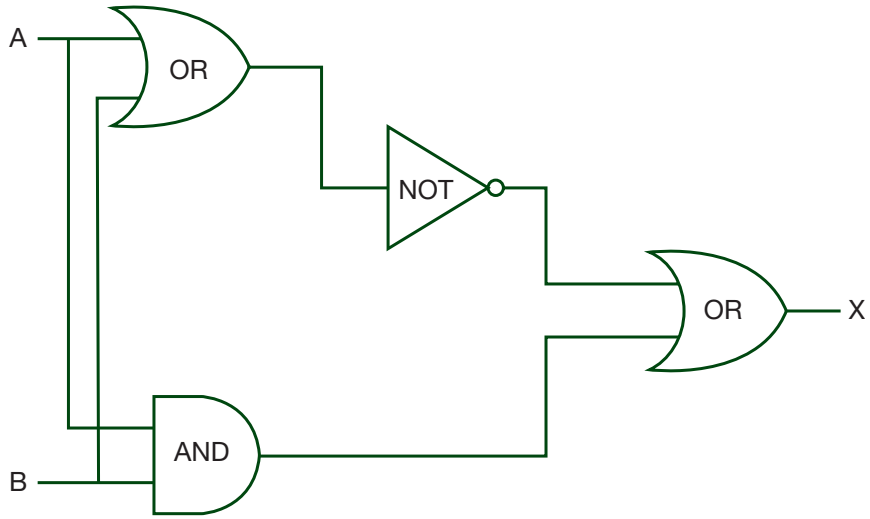
9.4 End of chapter questions

In questions 1 to 6 produce truth tables from the given logic circuits (networks). Remember, if there are two inputs then there will be 4 possible outputs; if there are three inputs then there will be 8 possible outputs.
The truth tables will look like this:

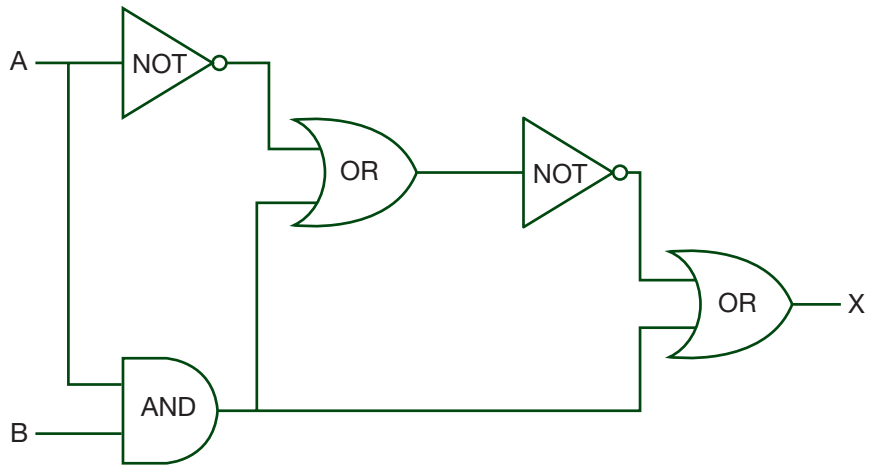
Input A	Input B	Output X
0	0	
0	1	
1	0	
1	1	

Input A	Input B	Input C	Output X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

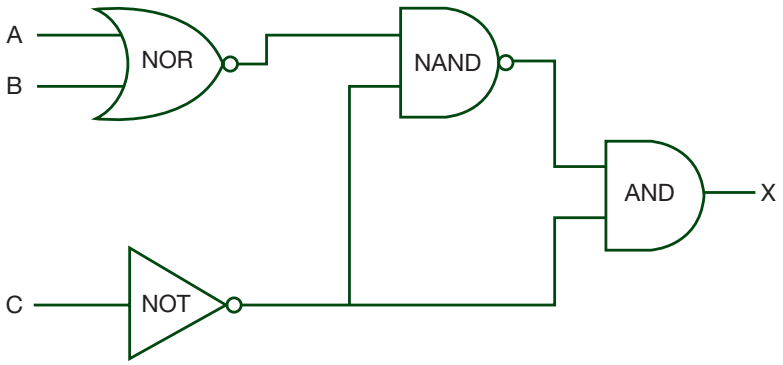
9.4.1



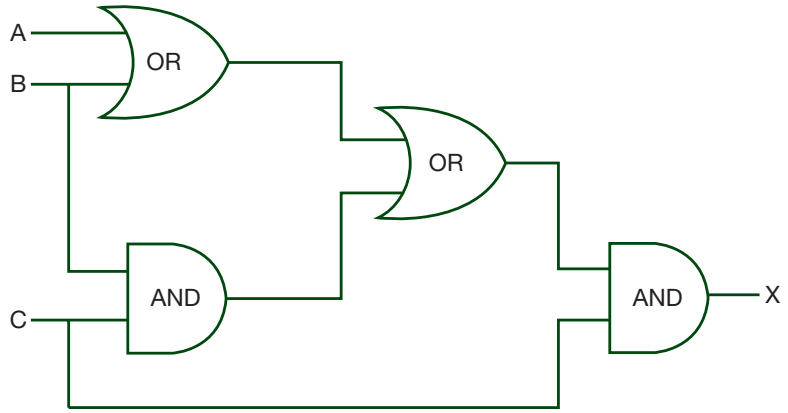
9.4.2



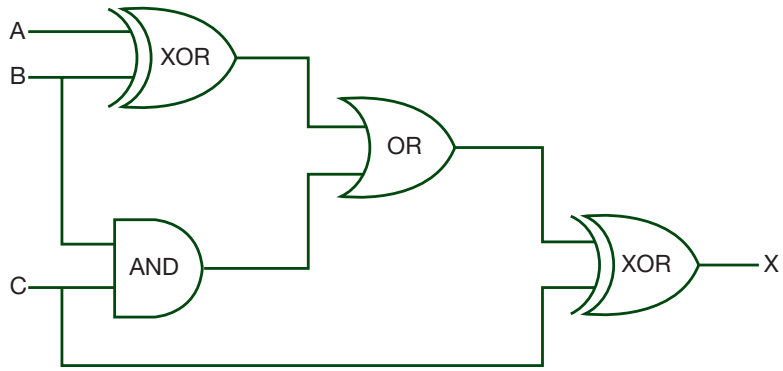
9.4.3



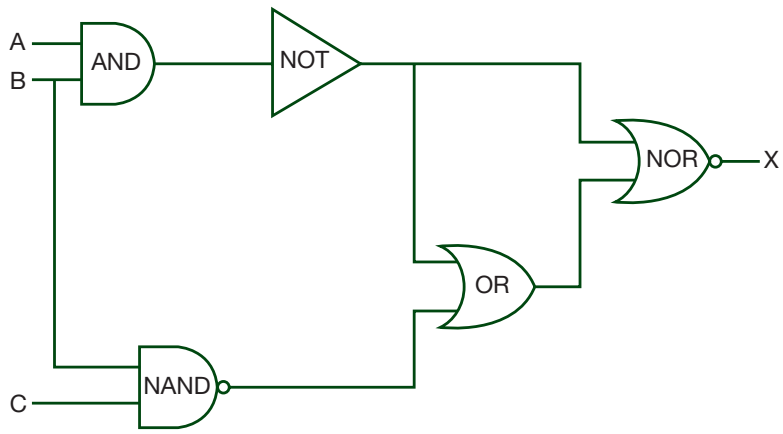
9.4.4



9.4.5



9.4.6



Questions 7 to 10 require both the logic circuit (network) and the truth table to be drawn. The truth table can be derived from the logic circuit (network), but can also be derived from the original problem. This could therefore be used as a cross-check that the logic circuit (network) is a correct representation of the original problem.

9.4.7 An electronic system will only operate if three switches P, S and T are correctly set. An output signal (X = 1) will occur if R and S are both in the ON position **or** if R is in the OFF position and S and T are both in the ON position.

Design a logic circuit (network) to represent the above situation and also draw the truth table.

9.4.8 A traffic light system uses logic gates as part of the control system. The system is operated when the output D has the value 1. This happens when:

either (a) signal A is red

or (b) signal A is green and signals B and C are both red

(NOTE: You may assume for this problem that red = 0 and green = 1).

Design a logic circuit (network) and draw the truth table for the above system.

9.4.9 A chemical process gives out a warning signal (W = 1) when the process operates incorrectly. A logic circuit (network) is used to monitor the process and to determine whether W = 1.

Inputs	Binary values	Description of plant status
C	1	Chemical rate = 20 litres/second
	0	Chemical rate < 20 litres/second
T	1	Temperature = 91°C
	0	Temperature > 91°C
X	1	Concentration > 5M
	0	Concentration = 5M

A warning signal (W = 1) will be generated if:

either (a) Chemical rate < 20 litres/second

or (b) Temperature > 91°C and Concentration > 5M

or (c) Chemical rate = 20 litres/second and Temperature > 91C

Draw a logic circuit (network) and truth table to show all the possible situations when the warning signal could be received.

9.4.10 A nuclear power station has a safety system based on three inputs to a logic circuit (network). A warning signal (S = 1) is produced when certain conditions in the nuclear power station occur based on these three inputs.

Inputs	Binary values	Description of plant status
T	1	Temperature > 115°C
	0	Temperature <= 115°C
P	1	Reactor pressure > 15 bar
	0	Reactor pressure <= 15 bar
W	1	Cooling water > 120 litres/hour
	0	Cooling water <= 120 litres/ hour

A warning signal (S = 1) will be produced when any of the following occurs:

either (a) Temperature > 115°C and Cooling water <= 120 litres/ hour

or (b) Temperature <= 115°C and Reactor pressure > 15 bar or Cooling water <= 120 litres/hour

Draw a logic circuit (network) and truth table to show all the possible situations when the warning signal (S) could be received.